KEITHLEY

KPCMCIA-8AOU/B

8-Channel Analog Output with Digital I/O Data Acquisition Adapter User's Manual

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4/02

KPCMCIA-8AOU/B
8-Channel Analog Output with Digital I/O Data Acquisition Adapter
User's Manual

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The print history shown below lists the printing dates of all Revisions and Addenda created for this manual. The Revision Level letter increases alphabetically as the manual undergoes subsequent updates. Addenda, which are released between Revisions, contain important change information that the user should incorporate immediately into the manual. Addenda are numbered sequentially. When a new Revision is created, all Addenda associated with the previous Revision of the manual are incorporated into the new Revision of the manual. Each new Revision includes a revised copy of this print history page.

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Safety Precautions

The following safety precautions should be observed before using this product and any associated instrumentation. Although some instruments and accessories would normally be used with non-hazardous voltages, there are situations where hazardous conditions may be present.

This product is intended for use by qualified personnel who recognize shock hazards and are familiar with the safety precautions required to avoid possible injury. Read and follow all installation, operation, and maintenance information carefully before using the product. Refer to the manual for complete product specifications.

If the product is used in a manner not specified, the protection provided by the product may be impaired.

The types of product users are:

Responsible body is the individual or group responsible for the use and maintenance of equipment, for ensuring that the equipment is operated within its specifications and operating limits, and for ensuring that operators are adequately trained.

Operators use the product for its intended function. They must be trained in electrical safety procedures and proper use of the instrument. They must be protected from electric shock and contact with hazardous live circuits.

Maintenance personnel perform routine procedures on the product to keep it operating properly, for example, setting the line voltage or replacing consumable materials. Maintenance procedures are described in the manual. The procedures explicitly state if the operator may perform them. Otherwise, they should be performed only by service personnel.

Service personnel are trained to work on live circuits, and perform safe installations and repairs of products. Only properly trained service personnel may perform installation and service procedures.

Keithley products are designed for use with electrical signals that are rated Installation Category I and Installation Category II, as described in the International Electrotechnical Commission (IEC) Standard IEC 60664. Most measurement, control, and data I/O signals are Installation Category I and must not be directly connected to mains voltage or to voltage sources with high transient over-voltages. Installation Category II connections require protection for high transient over-voltages often associated with local AC mains connections. Assume all measurement, control, and data I/O connections are for connection to Category I sources unless otherwise marked or described in the Manual.

Exercise extreme caution when a shock hazard is present. Lethal voltage may be present on cable connector jacks or test fixtures. The American National Standards Institute (ANSI) states that a shock hazard exists when voltage levels greater than 30V RMS, 42.4V peak, or 60VDC are present. **A good safety practice is to expect that hazardous voltage is present in any unknown circuit before measuring.**

Operators of this product must be protected from electric shock at all times. The responsible body must ensure that operators are prevented access and/or insulated from every connection point. In some cases, connections must be exposed to potential human contact. Product operators in these circumstances must be trained to protect themselves from the risk of electric shock. If the circuit is capable of operating at or above 1000 volts, **no conductive part of the circuit may be exposed.**

Do not connect switching cards directly to unlimited power circuits. They are intended to be used with impedance limited sources. NEVER connect switching cards directly to AC mains. When connecting sources to switching cards, install protective devices to limit fault current and voltage to the card.

Before operating an instrument, make sure the line cord is connected to a properly grounded power receptacle. Inspect the connecting cables, test leads, and jumpers for possible wear, cracks, or breaks before each use.

When installing equipment where access to the main power cord is restricted, such as rack mounting, a separate main input power disconnect device must be provided, in close proximity to the equipment and within easy reach of the operator.

For maximum safety, do not touch the product, test cables, or any other instruments while power is applied to the circuit under test. ALWAYS remove power from the entire test system and discharge any capacitors before: connecting or disconnecting cables or jumpers, installing or removing switching cards, or making internal changes, such as installing or removing jumpers.

Do not touch any object that could provide a current path to the common side of the circuit under test or power line (earth) ground. Always make measurements with dry hands while standing on a dry, insulated surface capable of withstanding the voltage being measured.

The instrument and accessories must be used in accordance with its specifications and operating instructions or the safety of the equipment may be impaired.

Do not exceed the maximum signal levels of the instruments and accessories, as defined in the specifications and operating information, and as shown on the instrument or test fixture panels, or switching card.

When fuses are used in a product, replace with same type and rating for continued protection against fire hazard.

Chassis connections must only be used as shield connections for measuring circuits, NOT as safety earth ground connections.

If you are using a test fixture, keep the lid closed while power is applied to the device under test. Safe operation requires the use of a lid interlock.

If  or  is present, connect it to safety earth ground using the wire recommended in the user documentation.

The  symbol on an instrument indicates that the user should refer to the operating instructions located in the manual.

The  symbol on an instrument shows that it can source or measure 1000 volts or more, including the combined effect of normal and common mode voltages. Use standard safety precautions to avoid personal contact with these voltages.

The **WARNING** heading in a manual explains dangers that might result in personal injury or death. Always read the associated information very carefully before performing the indicated procedure.

The **CAUTION** heading in a manual explains hazards that could damage the instrument. Such damage may invalidate the warranty.

Instrumentation and accessories shall not be connected to humans.

Before performing any maintenance, disconnect the line cord and all test cables.

To maintain protection from electric shock and fire, replacement components in mains circuits, including the power transformer, test leads, and input jacks, must be purchased from Keithley Instruments. Standard fuses, with applicable national safety approvals, may be used if the rating and type are the same. Other components that are not safety related may be purchased from other suppliers as long as they are equivalent to the original component. (Note that selected parts should be purchased only through Keithley Instruments to maintain accuracy and functionality of the product.) If you are unsure about the applicability of a replacement component, call a Keithley Instruments office for information.

To clean an instrument, use a damp cloth or mild, water based cleaner. Clean the exterior of the instrument only. Do not apply cleaner directly to the instrument or allow liquids to enter or spill on the instrument. Products that consist of a circuit board with no case or chassis (e.g., data acquisition board for installation into a computer) should never require cleaning if handled according to instructions. If the board becomes contaminated and operation is affected, the board should be returned to the factory for proper cleaning/servicing.

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1
Introduction

General information

The KPCMCIA-8AO is an 8-channel analog output adapter for systems equipped with a type II PCMCIA slot. Two versions of the adapter are available:

- KPCMCIA-8AOU
- KPCMCIA-8AOB

KPCMCIA-8AOU

- Eight independent unipolar analog outputs.
- Output voltages from 0 to +5V in 1.22mV increments.

KPCMCIA-8AOB

- Eight independent bipolar analog outputs.
- Output voltages from -5 to +5V in 2.44mV increments.

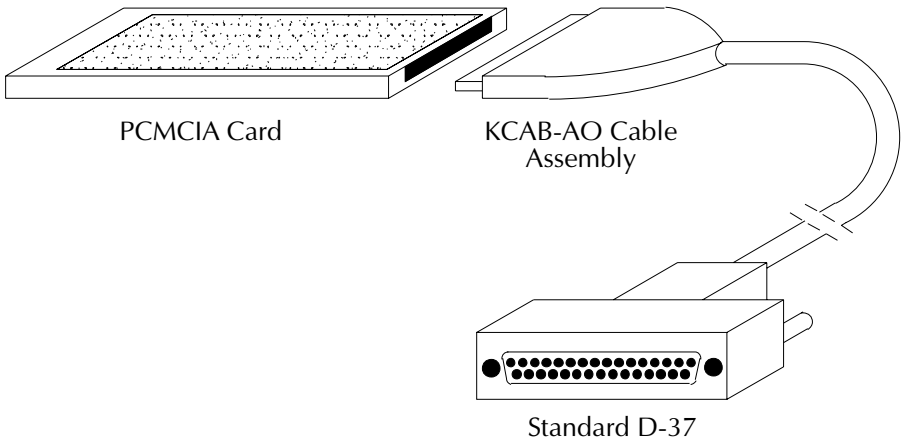
Features common to both adapter versions include:

- 12-bit resolution.
- Less than 10µs settling time to 1/2 LSB (Least Significant Byte).
- 1mA output current on each analog channel.
- Simultaneous output on two to eight channels.
- Eight bits of digital I/O individually programmable as input or output.
- On-board event timer to control output data rates.
- External interrupt input.

NOTE *Throughout this manual, any reference to the KPCMCIA-8AO refers to information common to both the U and the B versions.*

Figure 1-1 illustrates a complete system. If you do not want to interface to the KPCMCIA-8AO's 0.8mm, I/O connector, an adapter cable is provided to convert this connector into an industry-standard D-37 male connector. For applications requiring discrete wire hook-ups, an optional screw terminal adapter is available to convert the D-37 connector into 37 discrete screw terminal blocks.

Figure 1-1
KPCMCIA-8AO card and KCAB-AO cable assembly



Technical support

Before returning any equipment for repair, call Keithley Instruments, Inc., for technical support at:

1-888-KEITHLEY
Monday - Friday, 8:00 a.m. - 5:00 p.m., Eastern Time

An applications engineer will help you diagnose and resolve your problem over the telephone.

If a telephone resolution is not possible, the applications engineer will issue you a Return Material Authorization (RMA) number and ask you to return the equipment. Include the RMA number with any documentation regarding the equipment.

When returning equipment for repair, include the following information:

- Your name, address, and telephone number.
- The invoice or order number and date of equipment purchase.
- A description of the problem or its symptoms.
- The RMA number on the **outside** of the package.

Repackage the equipment using the original anti-static wrapping, if possible, and handle it with ground protection. Ship the equipment to:

ATTN: RMA #_____
Repair Department
Keithley Instruments, Inc.
28775 Aurora Road
Cleveland, OH 44139

Telephone 1-888-KEITHLEY
FAX (440) 248-6168

NOTES *If you are submitting your equipment for repair under warranty, you must include the invoice number and date of purchase.*

To enable Keithley Instruments, Inc., to respond as quickly as possible, you must include the RMA number on the outside of the package.

2
Installation

A Windows 95 INF configuration file has been written for the KPCMCIA-8AO hardware.

Hardware installation

To physically install the KPCMCIA-8AOU/B PC card, insert the card into an available Type II KPCMCIA socket.

Software setup

Refer to your DriverLINX documentation for a detailed description of the software installation and setup procedures.

3
Theory of Operation

Analog outputs

The KPCMCIA-8AO is constructed with four dual-channel, 12-bit, serial load, D/A converters. The D/A converters may be written using 8 or 16-bit I/O instructions, although 16-bit instructions are recommended. If 8-bit I/O transfers are used, the least significant byte (LSB) must be written before the most significant byte (MSB) as the contents of the data register are transferred to the appropriate D/A converter after the MSB is written.

Approximately 8µs is required to transfer the data into the D/A converter, and no D/A converter may be written to until this transfer is complete. During non-simultaneous output operations, the analog output of the D/A converter begins changing as soon as all of the data bits are received and settles to less than 1/2 LSB of the final value within 10µs under all conditions.

The analog outputs of the KPCMCIA-8AO are each rated for 1mA of load current. The total analog output current must remain less than 12mA, or damage to the KPCMCIA-8AO may result.

CAUTION The KPCMCIA-8AO may be permanently damaged if the total load on the analog outputs exceeds 12mA or if individual channel load exceeds 1mA.

Data formats

The bipolar KPCMCIA-8AOB uses 2's complement digital codes ranging from -2048 to +2047 (see Table 3-1). The unipolar KPCMCIA-8AOU uses straight binary digital input codes ranging from 0 to 4095 (see Table 3-2). Both adapters reset to 0 volts on power-up and after a software reset.

Table 3-1
KPCMCIA-8AOB data format

Vout = (Value / 4096) × 10													
Value	**Data bits DA11 ... DA0**												**Output**
-2048	1	0	0	0	0	0	0	0	0	0	0	0	-5.00000
-1	1	1	1	1	1	1	1	1	1	1	1	1	-0.00244
0	0	0	0	0	0	0	0	0	0	0	0	0	0.00000
1	0	0	0	0	0	0	0	0	0	0	0	1	0.00244
2047	0	1	1	1	1	1	1	1	1	1	1	1	4.99756

Table 3-2
KPCMCIA-8AOU data format

Vout = (Value / 4096) × 5													
Value	**Data bits DA11 ... DA0**												**Output**
0	0	0	0	0	0	0	0	0	0	0	0	0	0.00000
1	0	0	0	0	0	0	0	0	0	0	0	1	0.00122
2047	0	1	1	1	1	1	1	1	1	1	1	1	2.49878
2048	1	0	0	0	0	0	0	0	0	0	0	0	2.50000
4095	1	1	1	1	1	1	1	1	1	1	1	1	4.99878

Simultaneous analog output

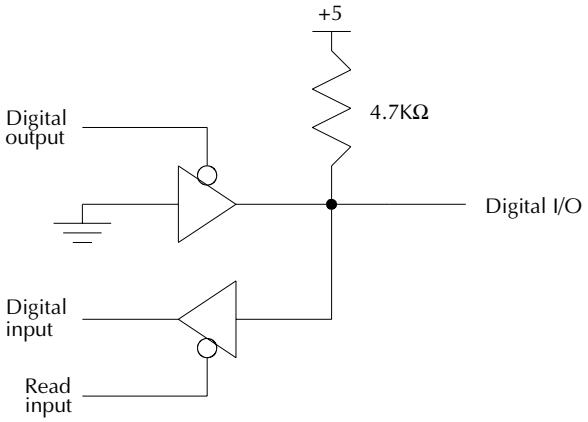
The KPCMCIA-8AO is capable of simultaneous output on two through eight analog outputs. To perform simultaneous output, the associated simultaneous load bit(s) in the KPCMCIA-8AO's simultaneous output register must be set to logic 1 before any data is written to the D/A converters. As long as a channel's simultaneous load bit is set to logic 1, any data written to that D/A converter is held in an internal data buffer and is not converted to an analog output voltage. After all of the D/A channels have been written, the analog outputs may be updated simultaneously by clearing the simultaneous load bits. The simultaneous load bits may be cleared under software control by writing logic 0s to the associated bit locations or under hardware control by generating a low-to-high transition on the external load control input (pin 30 on the I/O connector).

Digital input/output

The KPCMCIA-8AO is equipped with eight bits of digital I/O that may be individually programmed as input or output. To use a digital I/O bit as an output, set the corresponding bit in the KPCMCIA-8AO's digital I/O register to a logic 0 or logic 1 for the desired output value. To use a digital I/O bit as an input, the corresponding bit in the digital I/O register must be set to logic 1.

All of the digital I/O bits are reset to the input mode upon power-up and after a hardware reset. Each digital input is equipped with a 4.7KΩ pull-up resistor and will read a logic 1 if disconnected. Refer to Figure 3-1.

Figure 3-1
Basic KPCMCIA-8AO digital I/O schematic



Each digital output is capable of sinking 4mA. The output source current is provided by a 4.7kΩ pull-up resistor on each output bit resulting in approximately 1mA of output current. If additional drive current is required, a 2kΩ or larger pull-up resistor may be connected externally to the KPCMCIA-8AO.

Timer

The KPCMCIA-8AO is equipped with an event timer to pace events under CPU or interrupt control. The timer circuit features an 8-bit software programmable timer that counts the output of a selectable pre-scaler. The timer counts at a rate of 100kHz (100µs) or 1kHz (1ms) resulting in timer output rates ranging from 50kHz to 4Hz (200µs to 250ms).

Whenever the timer expires, a timer event and/or an optional timer interrupt (if used) are generated. This event and/or interrupt may be monitored by software to pace other operations. The timer output is also available on pin 27 of the I/O connector as a TTL level signal going high (logic 1) for one count each time the timer expires.

D/A loading

The D/A loading signal is a TTL level output available on pin 28 of the I/O connector. D/A loading changes to a logic 0 state while data transfers to one of the eight D/A converters and returns to a logic 1 when the transfer is complete.

If the D/A converter being written is not configured for simultaneous output mode, its analog output begins to update to its new voltage level when the D/A loading signal makes the low-to-high transition. The analog output settles to within 1/2 LSB of this low-to-high transition.

If the D/A converter being written is configured for simultaneous output mode, D/A loading may be used to determine when the transfer is complete so the external load control input does not occur until the data transfer is complete.

External load control

The external load control signal is a TTL-compatible input on pin 30 of the I/O connector and may be used to control the loading of the D/A converters configured for simultaneous output mode. A low-to-high transition of the external load control input clears all of the simultaneous load bits in the KPCMCIA-8AO's load control register. This causes any D/A converters configured for simultaneous output operation to update their analog output(s). The load event and the optional load event interrupt are also generated by the low-to-high transition of this input.

The external load control input is equipped with a 4.7kΩ pull-up resistor and may be disconnected when not in use.

External event

The KPCMCIA-8AO offers a TTL-compatible external event input on pin 31 of the I/O connector that uses the CPU to monitor external hardware events. The external event and the optional external event interrupt are generated by a low-to-high transition of this input.

The external event input is equipped with a 4.7kΩ pull-up resistor and may be disconnected when not in use.

4
Register Descriptions

Introduction

The KPCMCIA-8AO uses eight consecutive I/O locations within the I/O address map of the system. The base address of the adapter is determined by the client driver or enabler software programs as discussed in Section 3. The next eight I/O locations are used by the KPCMCIA-8AO for the functions listed in Table 4-1. Each register of the KPCMCIA-8AO is discussed in detail in the following paragraphs.

Table 4-1
KPCMCIA-8AO register descriptions

A2	A1	A0	I/O address	Register description
0	0	0	base address + 0	D/A converter data - LSB
0	0	1	base address + 1	D/A converter data - MSB
0	1	0	base address + 2	Control register
0	1	1	base address + 3	Simultaneous output register
1	0	0	base address + 4	Timer register
1	0	1	base address + 5	Digital I/O
1	1	0	base address + 6	Interrupt register
1	1	1	base address + 7	Reserved for future use

D/A converter data (LSB, MSB)

The D/A converter data register, located at base address + 0 and base address + 1, is used to output data to one of the D/A converters. Sixteen-bit I/O transfers should be used to access this register. If 8-bit I/O transfers are used, the LSB register must be written before the MSB register because the contents of the data register are transferred to the D/A converter when the MSB register is written. After the MSB register is written, approximately 8µs is required to transfer the contents of the data register into the D/A converter. The data register must not be written to during this interval. The READY bit, located in the control register, can be used to determine when data can be safely written to the data register. The data register can be read at any time and returns the last value written.

The format of the data written to the data register is:

	D7	D6	D5	D4	D3	D2	D1	D0
MSB	0	C2	C1	C0	DA11	DA10	DA9	DA8
LSB	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

where Cx selects the D/A converter:

	C2	C1	C0
DAC 0	0	0	0
DAC 1	0	0	1
DAC 2	0	1	0
DAC 3	0	1	1
DAC 4	1	0	0
DAC 5	1	0	1
DAC 6	1	1	0
DAC 7	1	1	1

and DAx represents the data bits transferred to the D/A converter:

Decimal	**Data bits DA11 ... DA0**												**B**	**U**
-2048	1	0	0	0	0	0	0	0	0	0	0	0	-5.00000	n/a
-1	1	1	1	1	1	1	1	1	1	1	1	1	-0.00244	n/a
0	0	0	0	0	0	0	0	0	0	0	0	0	0.00000	0.00000
1	0	0	0	0	0	0	0	0	0	0	0	1	0.00244	0.00122
2047	0	1	1	1	1	1	1	1	1	1	1	1	4.99756	2.49878
2048	1	0	0	0	0	0	0	0	0	0	0	0	n/a	2.50000
4095	1	1	1	1	1	1	1	1	1	1	1	1	n/a	4.99878

Control register

The control register, located at base address + 2, is used to control the KPCMCIA-8AO's event timer and interrupt selections. Upon power-up, all bits in the control register are set to logic 0. Refer to Table 4-2.

Table 4-2
Control register bit descriptions

Bit	Name	Description
7	RESET	During write operations, setting this bit to logic 1 generates a hardware reset to the D/A converters and resets the analog outputs to 0V. RESET is self clearing.
	READY	During read operations, this bit indicates the status of the D/A converter control circuitry. When set to logic 1, the KPCMCIA-8AO is ready and data may be safely written to the D/A converter data register. When set to logic 0, the KPCMCIA-8AO transfers the contents of the data register to one of the D/A converters. The data register must not be written while READY = 0.
6	Reserved	This bit returns a logic 0 during read operations and must be set to logic 0 for write operations.
5	TIMER_EVENT	During read operations, a logic 1 indicates the event timer has expired at least once since TIMER_EVENT was last reset. An interrupt can be generated from TIMER_EVENT by setting the TIMER_IRQ_EN bit in the KPCMCIA-8AO's interrupt register. TIMER_EVENT is reset by writing a logic 1 to this bit location or by halting the event timer (setting TIMER_RUN = 0).
4	EXT_EVENT	During read operations, a logic 1 indicates at least one low-to-high transition of the external event input (pin 31 of the I/O connector) has occurred since EXT_EVENT was last reset. An interrupt may be generated from EXT_EVENT by setting the EXT_IRQ_EN bit in the KPCMCIA-8AO's interrupt register. EXT_EVENT is reset by writing a logic 1 to this bit location.
3	Reserved	This bit returns a logic 0 during read operations and must be set to logic 0 for write operations.
2	Reserved	This bit returns a logic 0 during read operations and must be set to logic 0 for write operations.
1	TIMER_SOURCE	When set to logic 1, the event timer operates from a 100kHz clock source (100µs per count). When set to logic 0, the event timer operates from a 1kHz clock source (1ms per count).
0	TIMER_RUN	When set to logic 1, this bit enables the operation of the event timer. When set to logic 0, the timer is disabled.

Simultaneous output register

The simultaneous output register, located at base address + 3, is used to control the simultaneous output capabilities of the KPCMCIA-8AO. Upon power-up, all bits in the load register are set to logic 0. Refer to Table 4-3.

Table 4-3
Simultaneous output register bit descriptions

Bit	Name	Description
7	Reserved	This bit returns a logic 0 during read operations and must be set to logic 0 for write operations.
6	Reserved	This bit returns a logic 0 during read operations and must be set to logic 0 for write operations.
5	Reserved	This bit returns a logic 0 during read operations and must be set to logic 0 for write operations.
4	LOAD_EVENT	During read operations, a logic 1 indicates at least one low-to-high transition of the external load control input (pin 30 of the I/O connector) has occurred since LOAD_EVENT was last reset. An interrupt may be generated from LOAD_EVENT by setting the LOAD_IRQ_EN bit in the KPCMCIA-8AO's interrupt control register. LOAD_EVENT is cleared by writing a logic 1 to this bit location.
3	LOAD_67	When set to logic 1, D/A converter channels 6 and 7 are configured for simultaneous output and any data written to their data registers is not converted to an analog output. Clearing LOAD_67 to logic 0 returns D/A channels 6 and 7 to the standard operating mode and causes the last value output to each of their data registers to be converted to an analog output. A low-to-high transition of the external load control input (pin 30 of the I/O connector) also clears LOAD_67 to logic 0. Additional information on simultaneous output operation is available in Section 3.
2	LOAD_45	When set to logic 1, D/A converter channels 4 and 5 are configured for simultaneous output and any data written to their data registers is not converted to an analog output. Clearing LOAD_45 to logic 0 returns D/A channels 4 and 5 to the standard operating mode and causes the last value output to each of their data registers to be converted to an analog output. A low-to-high transition of the external load control input (pin 30 of the I/O connector) also clears LOAD_45 to logic 0. Additional information on simultaneous output operation is available in Section 3.
1	LOAD_23	When set to logic 1, D/A converter channels 2 and 3 are configured for simultaneous output and any data written to their data registers is not converted to an analog output. Clearing LOAD_23 to logic 0 returns D/A channels 2 and 3 to the standard operating mode and causes the last value output to each of their data registers to be converted to an analog output. A low-to-high transition of the external load control input (pin 30 of the I/O connector) also clears LOAD_23 to logic 0. Additional information on simultaneous output operation is available in Section 3.

Table 4-3
Simultaneous output register bit descriptions (cont.)

0	LOAD_01	When set to logic 1, D/A converter channels 0 and 1 are configured for simultaneous output and any data written to their data registers is not converted to an analog output. Clearing LOAD_01 to logic 0 returns D/A channels 0 and 1 to the standard operating mode and causes the last value output to each of their data registers to be converted to an analog output. A low-to-high transition of the external load control input (pin 30 of the I/O connector) also clears LOAD_01 to logic 0. Additional information on simultaneous output operation is available in Section 3.

Timer register

The timer register, located at base address + 4, is used to set the rate of the on-board event timer. Each time the timer expires, a timer event and an optional timer interrupt, if used, are generated (see "Control register" and "Interrupt register"). This event and/or interrupt can be monitored by software to pace other operations. The output of the timer is also available on pin 27 of the I/O connector.

The value written to the timer register determines the number of input clock cycles required before the timer expires and must be in the range 1 ≤ timer register value ≤ 255. A read of the timer register returns the last value written. The timer's output rate, which is equal to the timer's event rate, may be calculated using the equations:

$$\text{output rate (Hz)} = \frac{\text{input clock rate (Hz)}}{\text{register value} + 1}$$

- or -

$$\text{output rate (sec)} = \text{input clock rate (sec)} * (\text{register value} + 1)$$

where the timer's input clock rate is set to 100kHz (10µs per count) or 1kHz (1ms per count) using the TIMER_SOURCE bit located in the control register.

Upon power-up, the timer register is initialized to 0. A valid timer register value must be written to this register before the timer is enabled.

Digital I/O

The digital I/O register, located at base address + 5, directly controls the digital I/O signals on the output connector. To use a digital I/O bit as an output bit, write a logic 0 or a logic 1 to the associated location in the digital I/O register. To use a digital I/O bit as an input bit, a logic 1 must first be written to the associated bit in the digital I/O register. A read of the digital I/O register returns the current value of the digital inputs and the last value written to the digital outputs. Upon power-up, all digital I/O bits are set to input mode (logic 1).

Interrupt register

The interrupt register, located at base address + 6, is used to enable and disable interrupts and to determine the source of an interrupt during interrupt processing. Refer to Table 4-4.

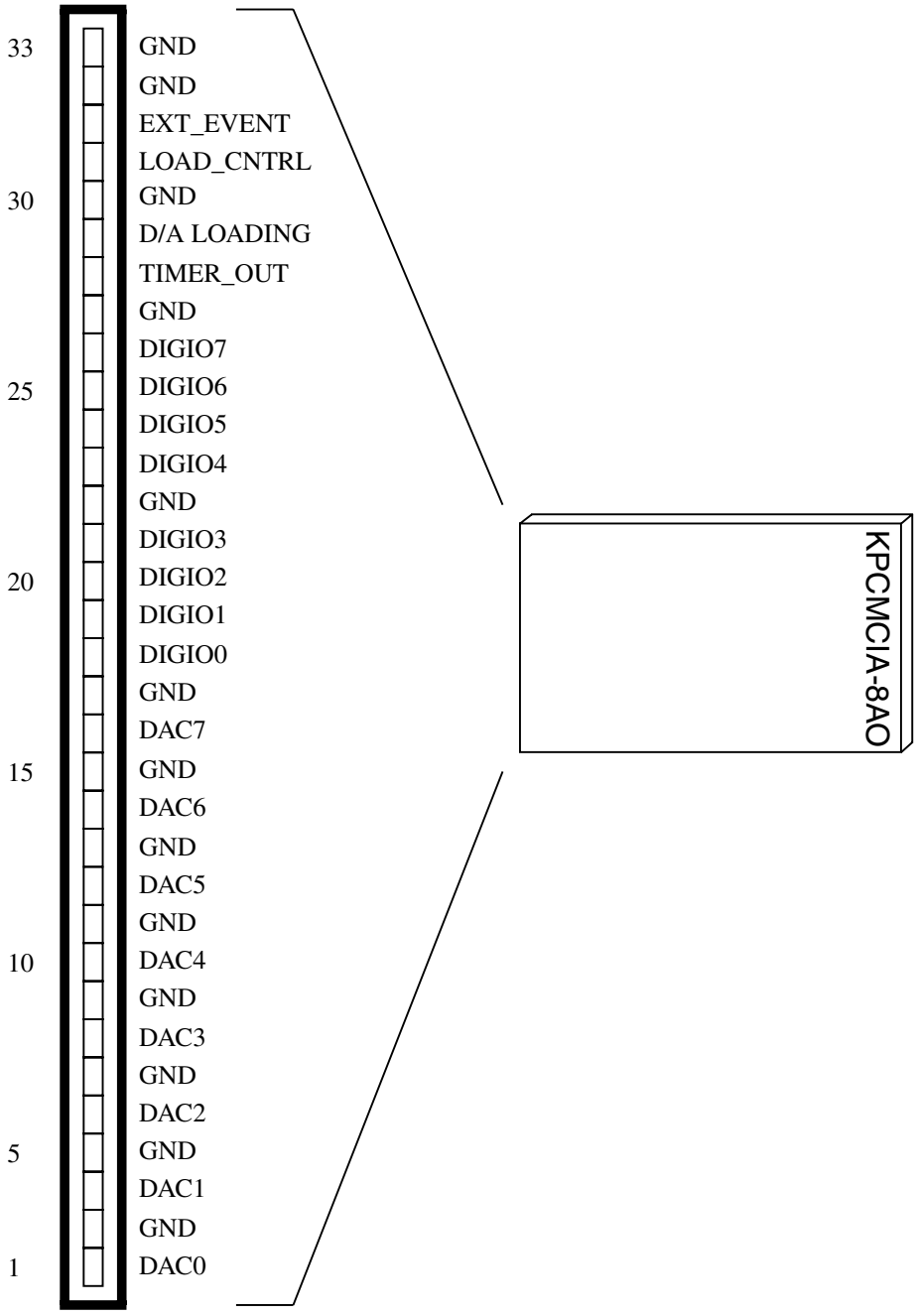
Table 4-4
Interrupt register bit descriptions

Bit	Name	Description
7	Reserved	This bit returns a logic 0 during read operations and must be set to logic 0 for write operations.
6	EXT_IRQ	During read operations, a logic 1 indicates an EXT_EVENT interrupt is pending. The external event interrupt must be disabled (EXT_IRQ_EN = 0) or the external event status must be reset (see EXT_EVENT in Table 4-2) before additional interrupts can be received. EXT_IRQ should be set to logic 0 during write accesses to this register.
5	LOAD_IRQ	During read operations, a logic 1 indicates a LOAD_EVENT interrupt is pending. The load event interrupt must be disabled (LOAD_IRQ_EN = 0) or the load event status must be reset (see LOAD_EVENT in Table 4-3) before additional interrupts can be received. LOAD_IRQ should be set to logic 0 during write accesses to this register.
4	TIMER_IRQ	During read operations, a logic 1 indicates a TIMER_EVENT interrupt is pending. The timer event interrupt must be disabled (TIMER_IRQ_EN = 0) or the timer event status must be reset (see TIMER_EVENT in Table 4-2) before additional interrupts can be received. TIMER_IRQ should be set to logic 0 during write accesses to this register.
3	Reserved	This bit returns a logic 0 during read operations and must be set to logic 0 for write operations.
2	EXT_IRQ_EN	When set to logic 1, an interrupt is generated on each occurrence of EXT_EVENT. (See EXT_EVENT in Table 4-2.) When set to logic 0, external event interrupts are disabled.
1	LOAD_IRQ_EN	When set to logic 1, an interrupt is generated on each occurrence of LOAD_EVENT. (See LOAD_EVENT in Table 4-3.) When set to logic 0, load event interrupts are disabled.
0	TIMER_IRQ_EN	When set to logic 1, an interrupt is generated on each occurrence of TIMER_EVENT. (See TIMER_EVENT in Table 4-2.) When set to logic 0, timer event interrupts are disabled.

5
I/O Connections

The KPCMCIA-8AO is fitted with a 33-pin, 0.8mm shielded connector with the pins assigned as shown in Figure 5-1.

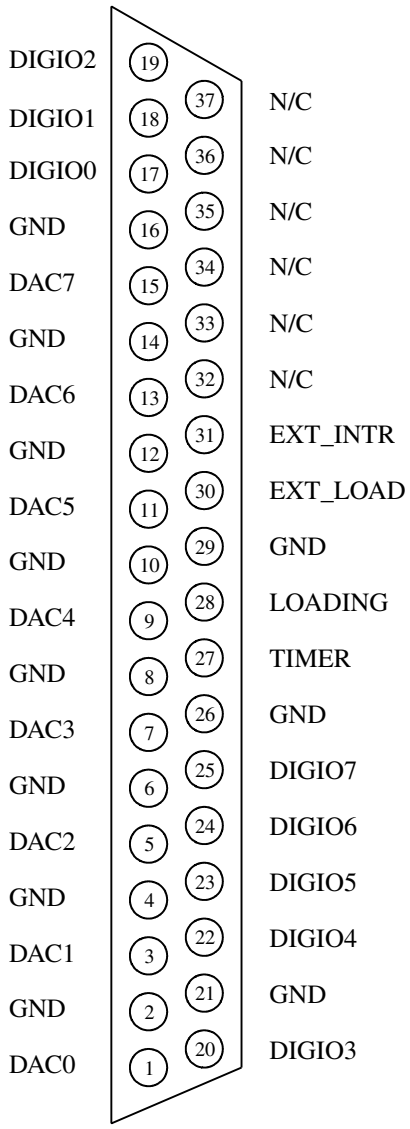
Figure 5-1
Output connector



KCAB-AO cable assembly

A cable assembly, Keithley part number KCAB-AO, is provided to convert the KPCMCIA-8AO's 33-pin, 0.8mm I/O connector to a standard D-37 male connector. The first 31 connections on the KPCMCIA-8AO map directly to the first 31 pins of the D-37 connector. Refer to Figure 5-2. Note that two of the KPCMCIA-8AO's ground connections (pins 32 and 33) are not available when using the KCAB-AO.

Figure 5-2
KPCMCIA-8AO output connections using the KCAB-AO



A
Specifications

Resolution	12 bits
Relative accuracy	±1 LSB maximum
Offset error	±5 LSB maximum (KPCMCIA-8AOU) ±6 LSB maximum (KPCMCIA-8AOB)
Full-scale error[1]	±6 LSB maximum
Settling time to ±1/2 LSB	
Positive full-scale change	10µs maximum (3µs typical)
Negative full-scale change	10µs maximum (5µs typical)
Glitch-impulse	30nV-sec typical
Digital feedthrough	10nV-sec typical
Digital crosstalk	10nV-sec typical
Output load current[2]	1mA per channel typical 12mA per adapter maximum
Power requirements	
No load	120mA @ +5V maximum
Full-rated load	140mA @ +5V maximum
Power-down mode	20mA @ +5V maximum

Specifications subject to change without notice.

[1]Full-scale error includes offset error.

[2]Total output load currents in excess of 12mA may result in damage to the KPCMCIA-8AOU/8AOB.

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Specifications are subject to change without notice.

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